



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of )  
K. Manetakis ) For: LOW-VOLTAGE CLASS-AB  
Serial No. 09/943,888 ) OUTPUT STAGE AMPLIFIER  
Filed: August 30, 2003 ) ) Group No. 2819

INFORMATION DISCLOSURE STATEMENT  
UNDER 37 CFR § 1.97(b)

Assistant Commissioner of Patents  
Alexandria, VA 22313

Dear Sir:

Applicants submit herewith references of which they are aware in accordance with 37 CFR § 1.56.

In accordance with 37 CFR § 1.98 submitted herewith for consideration by the Examiner are the patents, publications and other information shown on the attached PTO-1449.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on:

May 23, 2003

(Date of Deposit)

Victoria J. Pacey

(Name of the Person Making Deposit)



(Signature)

May 23, 2003

(Date of Signature)

(IDS\_US.VER1.1-9/13/01)

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The citation of these references is not intended to constitute an admission that any reference referred to herein is prior art to the invention of this application unless specifically designated as such.

The filing of this document shall not be construed to mean that any search has been made or, that if made, such search was complete or exhaustive, or that no other material information as defined in 37 CFR § 1.56 exists.

A list of the references cited herein is set forth on Form PTO-1449, which is enclosed herewith in duplicate along with a copy of each cited reference. Applicants respectfully request that the Examiner return to Applicants the enclosed copy of the Form PTO-1449 indicating consideration of the references.

These references are being submitted prior to the issuance of the first Office Action. Therefore, it is believed that no fee is due for this submission.

Respectfully submitted,

Dated: May 23, 2003

By:

  
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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE  
(REV. 7-80) PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT  
(Use several sheets if necessary)

DATE MAILED: May 23, 2003

ATTY. DOCKET NO. 010186 SERIAL NO. 09/943,888

APPLICANT  
K. Manetakis

FILING DATE August 30, 2001 GROUP 2819

U.S. PATENT DOCUMENTS

| EXAMINER INITIAL | Ref No | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE IF APPROPRIATE |
|------------------|--------|-----------------|------|------|-------|-----------|----------------------------|
|                  | A1     |                 |      |      |       |           |                            |
|                  | A2     |                 |      |      |       |           |                            |
|                  | A3     |                 |      |      |       |           |                            |
|                  | A4     |                 |      |      |       |           |                            |
|                  | A5     |                 |      |      |       |           |                            |
|                  | A6     |                 |      |      |       |           |                            |
|                  | A7     |                 |      |      |       |           |                            |
|                  | A8     |                 |      |      |       |           |                            |
|                  | A9     |                 |      |      |       |           |                            |

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FOREIGN PATENT DOCUMENTS

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|------------------|--------|-----------------|------|---------|------|-------|-----------|
|                  | B1     |                 |      |         |      |       |           |
|                  | B2     |                 |      |         |      |       |           |
|                  | B3     |                 |      |         |      |       |           |

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Page, Etc.)

|    |  |                                                                                                                                                                                                    |
|----|--|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C1 |  | Eric Vittoz, "Analog VLSI Signal Processing: Why, Where and How?", Journal of VLSI Signal Processing, Vol. 8, pps 27-44 and Analog Integrated Circuits and Signal Processing, pps 27-44, July 1994 |
| C2 |  | Yan ,et al., "Low Voltage Analog Circuit Design Techniques: A Tutorial", IEICE Trans. Analog Integrated Circuits and Systems, vol E00-A, No. 2, February 2000                                      |
| C3 |  |                                                                                                                                                                                                    |

EXAMINER DATE CONSIDERED

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.